WHAT IS CLAIMED IS:

1. A three dimension (3D) polysilicon read only memory (ROM), at least comprising:

a silicon substrate;

an isolated silicon dioxide (SiO_2) layer, which is deposited on the silicon substrate;

a N-Type heavily doped (N+) polysilicon layer, which is deposited on the isolated SiO_2 layer and is further defined a plurality of parallel, separate word lines (WL);

a first oxide layer, which is filled in the space between the word lines;

a dielectric layer, which is deposited on the word lines and the first oxide layer;

a P-Type lightly doped (P-) polysilicon layer, which is deposited on the dielectric layer and is further defined a plurality of parallel, separate bit lines (BL), wherein the bit lines overlap the word lines, from a top view, to form a shape approximately as a cross;

at least a neck structure, which are individually formed between the first

polysilicon layer and the second polysilicon layer by isotropy etching the dielectric layer and using dilute hydrofluoric acid (HF); and

a second oxide layer, which is filled in the space between the bit lines and is on the word lines and the first oxide layer.

2. The 3D polysilicon ROM according to claim 1, wherein the N-Type heavily doped (N+) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

3. The 3D polysilicon ROM according to claim 1, wherein the P-Type lightly doped (P-) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

4. The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the bit lines, respectively.

5. The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

6. The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

7. The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of a polymer.

8. The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of a low K material.

9. The 3D polysilicon ROM according to claim 1, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

10. A method of fabricating a 3D polysilicon ROM, comprising the steps of:

providing a substrate;

depositing an isolated SiO_2 layer on the substrate;

forming a first polysilicon layer on the isolated SiO_2 layer; patterning the first polysilicon layer to define a plurality of parallel, separate word lines (WL);

filling the space between the word lines to form a first oxide layer;

planarizing the first polysilicon layer and the first oxide layer to form a planarized surface;

forming a dielectric layer on the planarized surface;

forming a second polysilicon layer on the dielectric layer; patterning the second polysilicon layer to define a plurality of parallel, separate bit lines (BL), wherein the bit lines overlap the word lines, from a top view, to form a shape approximately as a cross;

isotropy etching the dielectric layer by wet etching, with using dilute hydrofluoric acid (HF), to form necks between the first polysilicon layer and the second polysilicon layer; and

forming a second oxide layer by filling oxides in the space between the bit lines and is on the word lines and the first oxide layer.

11. The method of fabricating a 3D polysilicon ROM according to claim 10, the first polysilicon layer is a N-Type heavily doped (N+) polysilicon layer, and the second polysilicon layer is a P-Type lightly doped (P-) polysilicon layer.

12. The method of fabricating a 3D polysilicon ROM according to claim 11, wherein the N-Type heavily doped (N+) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

13. The method of fabricating a 3D polysilicon ROM according to claim 11,

the P-Type lightly doped (P-) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

14. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the bit lines, respectively.

15. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

16. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

17. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the first oxide layer and the second oxide layer are made of a polymer.

18. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the first oxide layer and the second oxide layer are made of a low K material.

19. The method of fabricating a 3D polysilicon ROM according to claim 10, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

20. A 3D polysilicon ROM, at least comprising:

a silicon substrate;

depositing an isolated SiO_2 layer on the silicon substrate;

a plurality of parallel, separate word lines (WL), which are defined on the isolated SiO_2 layer;

a plurality of parallel, separate bit line (BL) sections, which are formed on the word lines separately;

a plurality of parallel, separate dielectric sections, which are formed below the BL sections one by one, each one being with respect to the BL sections thereon and all being on the word lines;

at least a neck structure, which are individually formed for the dielectric sections with respect to the bit lines thereon;

a first oxide layer, which is filled in the space between the word lines, in

the space between the BL sections, in the space between the dielectric sections, and is on the word lines;

a plurality of parallel, separate bit lines, which are defined on the BL sections and on the first oxide layer, wherein the bit lines overlap the word lines, from a top view, to form a shape approximately as a cross and the bit lines are electrically coupled to the BL sections thereabout; and

a second oxide layer, which is filled in the space between the bit lines and is on the first oxide layer over the word lines.

21. The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the bit lines, respectively.

22. The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

23. The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

24. The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of a polymer.

25. The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of a low K material.

26. The 3D polysilicon ROM according to claim 20, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

27. A method of fabricating a 3D polysilicon ROM, comprising the steps of:

providing a silicon substrate;

forming an isolated SiO_2 layer on the silicon substrate;

forming a first polysilicon layer on the isolated SiO_2 layer;

forming a dielectric layer on the first polysilicon layer;

forming a second polysilicon layer on the dielectric layer; patterning the second polysilicon layer to define a plurality of parallel, separate first bit lines (BL) and patterning the dielectric layer to define a plurality of parallel, separate dielectric rails, wherein the dielectric rails are formed below the first bit lines;

forming a plurality of parallel, separate bit line (BL) sections for each first bit line and forming a plurality of parallel, separate dielectric sections, wherein

the dielectric sections are formed below the BL sections one by one, each one being with respect to the BL sections thereon and all being on the word lines;

isotropy etching the dielectric sections by wet etching, with using dilute hydrofluoric acid (HF), to form necks between the first polysilicon layer and the second polysilicon layer;

filling in the space between the word lines, in the space between the BL sections, in the space between the dielectric sections, and is on the word lines, to form a first oxide layer;

forming a plurality of parallel, separate second bit lines on the BL sections and on the first oxide layer, wherein the second bit lines overlap the word lines, from a top view, to form a shape approximately as a cross and the second bit lines are electrically coupled to the BL sections thereabout; and

forming a second oxide layer by filling oxides in the space between the second bit lines and is on the first oxide layer over the word lines.

28. The method of fabricating a 3D polysilicon ROM according to claim 27, the first polysilicon layer is a N-Type heavily doped (N+) polysilicon layer, and the second polysilicon layer is a P-Type lightly doped (P-) polysilicon layer.

29. The method of fabricating a 3D polysilicon ROM according to claim 28, wherein the N-Type heavily doped (N+) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

30. The method of fabricating a 3D polysilicon ROM according to claim 28, the P-Type lightly doped (P-) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

31. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the bit lines, respectively.

32. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

33. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

34. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the first oxide layer and the second oxide layer are made of a

polymer.

35. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the first oxide layer and the second oxide layer are made of a low K material.

36. The method of fabricating a 3D polysilicon ROM according to claim 27, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

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